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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,579	10/09/2001	Dominik J. Schmidt		6017

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EXAMINER	
LY, ANH VU H	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,579	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	Anh-Vu H. Ly	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16-24* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Specification

2. The disclosure is objected to because of the following informalities: there are numerous missing periods at the end of the sentences and paragraphs, e.g., page 1, line 17; page 2, lines 3 and 16; page 3, line 7; etc...

Appropriate correction is required.

Claim Objections

3. Claim 5 is objected to because of the following informalities: in line 2, after "(FIFO)" and before "positioned", a word such as buffer, memory, or queue must be inserted, e.g., (FIFO) buffer, (FIFO) queue, or (FIFO) memory since "FIFO" only stands for first-in-first-out and it is unclear what being referred to as first-in-first-out.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the

international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6, 8-11, 16, and 18-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanian et al (US Pub 2002/0031166 A1). Hereinafter, referred to as Subramanian.

With respect to claim 1, Subramanian discloses a multi-mode wireless device on a single substrate (Fig. 1A), comprising:

an analog portion integrated on the substrate (Fig. 1B, interface conversion/sector combining 116), including:

a radio frequency front-end (pages 4-5, 47th paragraph, the interface conversion block 116 includes components such as **a radio frequency transceiver** and an analog to digital, A/D, converter coupled to each other in series) to receive an RF signal from an antenna (Fig. 1B, antenna 120); and

an analog to digital converter (ADC) coupled to the RF front-end to digitize the RF signal (pages 4-5, 47th paragraph, the interface conversion block 116 includes components such as a radio frequency transceiver and **an analog to digital, A/D, converter coupled to each other in series**); and

a digital portion integrated on the substrate (Fig. 1B, processors, 102a, 120b, 104, 112, memory 106 and 118, controller 110a), including:

a reconfigurable logic core coupled to the ADC (Fig. 1B, DSP/uP 112), the reconfigurable logic core to handle a plurality of wireless communication protocols (page 3, 39th paragraph, the signal processing functions 16, including the DSP/uP 112, shown have a configurable architecture that enables the device to operate using a wide variety of

communication protocols, including CDMA, 3GPP, TDMA, as well as anticipated future protocols);

one or more general-purpose processor cores coupled to the reconfigurable logic core (Fig. 1B, processors, 102a, 102b, 104); and

a memory array coupled to the reconfigurable logic core (Fig. 1B, memory 106 and 118 coupled to processor 112 via bus 126 and 130a).

With respect to claim 2, Subramanian discloses that wherein the protocol conforms to **one** or more of a GSM protocol, GPRS protocol, EDGE protocol and an 802.11A protocol (page 3, 39th paragraph, the signal processing functions 16, including the DSP/uP 112, shown have a configurable architecture that enables the device to operate using a wide variety of communication protocols, including CDMA, 3GPP, TDMA, as well as anticipated future protocols. Herein, GSM protocol employing TDMA).

With respect to claims 3 and 23, Subramanian discloses that wherein the reconfigurable logic core is to deliver data in parallel to the one or more general-purpose processor cores (page 19, 188th – 189th paragraphs and Fig. 5, data is delivered parallel to multiple processors by the Function A 504 or the processor 112. Herein, Function A 504 includes multiple sub functions that can be performed in series or parallel).

With respect to claim 4, Subramanian discloses that wherein the reconfigurable logic core is to deliver data in series to the one or more general-purpose processor cores (page 19, 188th –

189th paragraphs and Fig. 5, data is delivered in series to multiple processors by the Function A 504 or the processor 112. Herein, Function A 504 includes multiple sub functions that can be performed in series or parallel).

With respect to claim 6, Subramanian discloses that wherein at least one or the one or more general-purpose processor cores includes a multiply-accumulate (MAC) unit (Fig. 2B, a multiple-accumulate (MAC) block 236).

With respect to claims 8 and 18, Subramanian discloses that the wireless device further comprising a router coupled to the reconfigurable logic core, cellular radio core, and short-range wireless transceiver core (Fig. 2A, allocator 219 coupled to processor 112 and interface conversion/sector combining 116, Fig. 1B).

With respect to claim 9, Subramanian discloses that wherein the router further comprises an engine to track the destination of packets (page 21, 208th paragraph, the signal is assigned a data pump path on one or more independent processors by the allocator 219. Herein, the address of the signal must be examined to determine what processors it should be sent to) and send them in parallel through a plurality of separate pathways (Fig. 2A, parallel buses 206a and 206i for forwarding signals).

With respect to claim 10, Subramanian discloses that wherein the router is to send packets in parallel through a primary and a secondary communication channel (Fig. 2A, parallel

buses 206a and 206i for forwarding signals. Herein, bus 206a is primary bus and 206i is secondary bus, as considered by examiner).

With respect to claim 11, Subramanian discloses a portable computer system (Fig. 1B), comprising:

a processor (Fig. 1B, controller 114);

a multi-mode wireless device on a single substrate coupled to the processor (Fig. 1B), the device comprising:

an analog portion integrated on the substrate (Fig. 1B, interface conversion/sector combining 116), including:

a cellular radio core having an analog to digital converter (ADC) configured to receive a radio signal from an antenna (pages 4-5, 47th paragraph and Fig. 1, the interface conversion block 116 includes components such as a radio frequency transceiver and **an analog to digital, A/D, converter coupled to each other in series** and coupled to antenna 120), and

a short-range wireless transceiver core (pages 4-5, 47th paragraph, the interface conversion block 116 includes components such as **a radio frequency transceiver** and an analog to digital, A/D, converter coupled to each other in series) to receive an RF signal from an antenna (Fig. 1B, antenna 120); and

a digital portion integrated on the substrate (Fig. 1B, processors, 102a, 120b, 104, 112, memory 106 and 118, controller 110a), including:

a reconfigurable logic core coupled to the ADC (Fig. 1B, DSP/uP 112), the reconfigurable logic core configured to handle a plurality of wireless communication protocols

(page 3, 39th paragraph, the signal processing functions 16, including the DSP/uP 112, shown have a configurable architecture that enables the device to operate using a wide variety of communication protocols, including CDMA, 3GPP, TDMA, as well as anticipated future protocols);

one or more general-purpose processor cores coupled to the reconfigurable logic core (Fig. 1B, processors, 102a, 102b, 104); and

a memory array coupled to the reconfigurable logic core (Fig. 1B, memory 106 and 118 coupled to processor 112 via bus 126 and 130a).

With respect to claim 16, Subramanian discloses that wherein the reconfigurable logic core includes one or more DSPs (Fig. 1B, DSP/uP 112).

With respect to claim 19, Subramanian discloses that wherein the router is to de-correlate data (Fig. 2A, allocator 219 splitting data to multiple kernel planes 201a-i).

With respect to claim 20, Subramanian discloses that wherein the router is to de-correlate data into parallel streams that are not time-correlated (Fig. 2A, allocator 219 splitting data to multiple kernel planes 201a-i independently).

With respect to claim 21, Subramanian discloses an input recognizer embodied in a program storage device, said input recognizer configured to receive input from a user (Fig. 1B, configuration data inputted from a user are stored in a memory 118).

With respect to claim 22, Subramanian discloses that the reconfigurable logic core comprises a vector processor (Fig. 1B, DSP/uP 112).

With respect to claim 24, Subramanian discloses that wherein the digital portion comprises a reconfigurable processor core including the reconfigurable logic core and one or more general-purpose processor cores (Fig. 1B, the reconfigurable processor core including DSP/uP 112, processors 102a, 102b, 104).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 7, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al (US Pub 2002/0031166 A1) in view of Hartmann (US Patent No. 6,096,091).

With respect to claim 5, Subramanian discloses a memory positioned between the reconfigurable logic core and at least one of the one or more general-purpose processor cores (Fig. 1B, memory 106 positioned between processor 112 and processor 102a). Subramanian does not disclose that the memory is a FIFO memory. Hartmann discloses a FIFO buffer 120A positioned between the reconfigurable logic 110A and processor 150 (Fig. 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include

a FIFO buffer in Subramanian's system, as suggested Hartmann, to buffer data in a sequential order.

With respect to claims 7 and 17, Subramanian discloses one or more general-purpose processor cores (Fig. 1B, processors 102a, 102b, 104). Subramanian does not disclose a RISC processor. Hartmann discloses that the embedded processor 150 is RISC processor (col. 4, lines 47-54 and Fig. 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include RSIC processor in Subramanian's system, as suggested by Hartmann, to reduce delay since RISC processors operate on a very limited number of instructions.

Response to Arguments

6. Applicant's arguments with respect to claims 1-11 and 16-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H. Ly whose telephone number is 571-272-3175. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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